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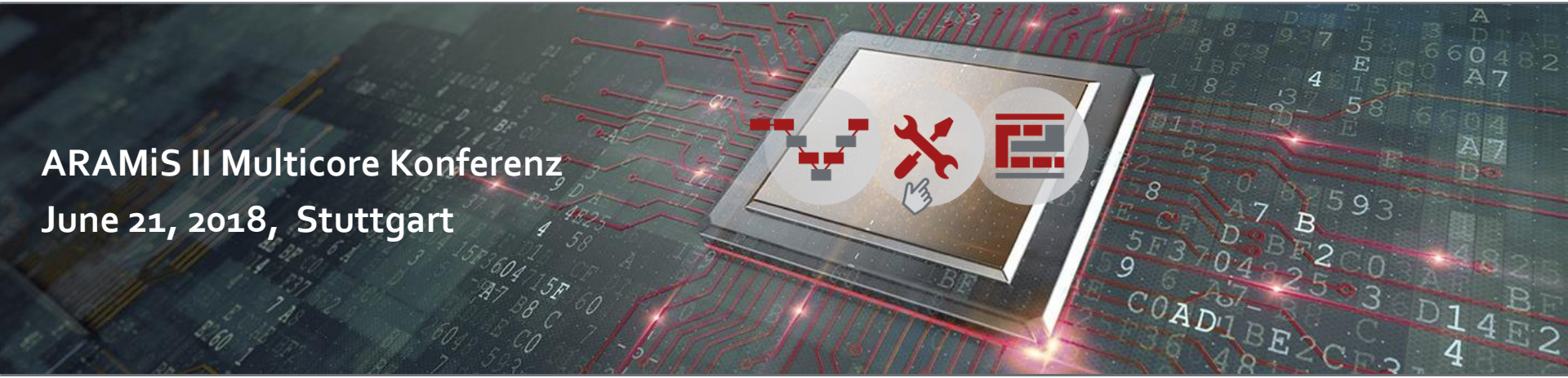
DEVELOPMENT PROCESSES I TOOLS I PLATFORMS
FOR SAFETY-CRITICIAL MULTICORE SYSTEMS



ARAMiS II Multicore Konferenz
June 21, 2018, Stuttgart

Efficient Toolchain for Multicore Processors on Aircraft Engine Controls

Dr. Alexander Walsch, GE Aviation

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Federal Ministry of Education and Research

GE Aviation

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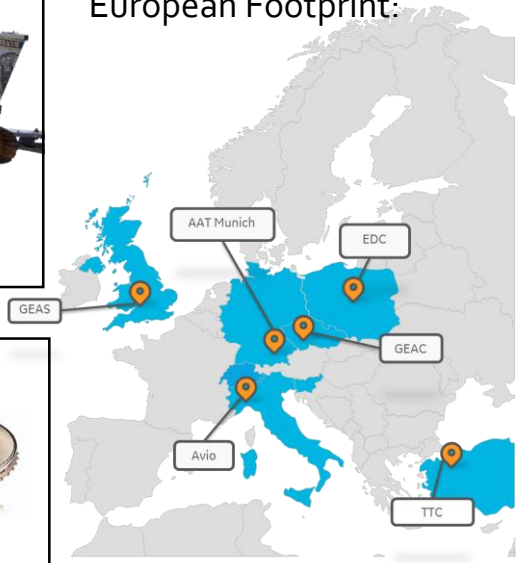
DEVELOPMENT PROCESSES I TOOLS I PLATFORMS
FOR SAFETY-CRITICIAL MULTICORE SYSTEMS

Commercial engines

Commercial engine services

Military engines and services

European Footprint:



BGA and Integrated Systems

- ✓ General aviation engines
- ✓ Power, mechanical, electronics

Avionics and Digital Systems

taleris

- ✓ Avionics
- ✓ Digital Services

Avio Aero

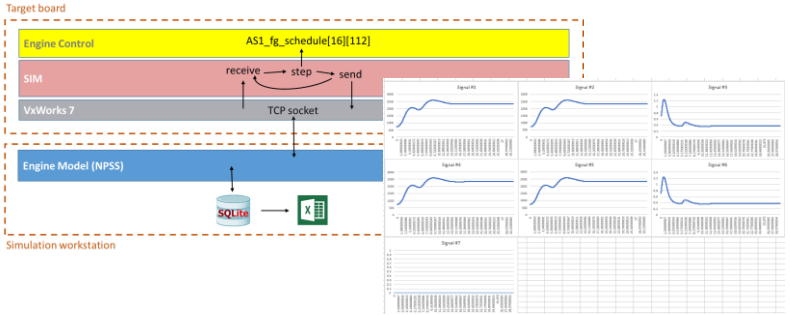
A GE Aviation Business

- ✓ Power Transmissions
- ✓ Turbo machinery

A leading provider of jet engines, systems and services

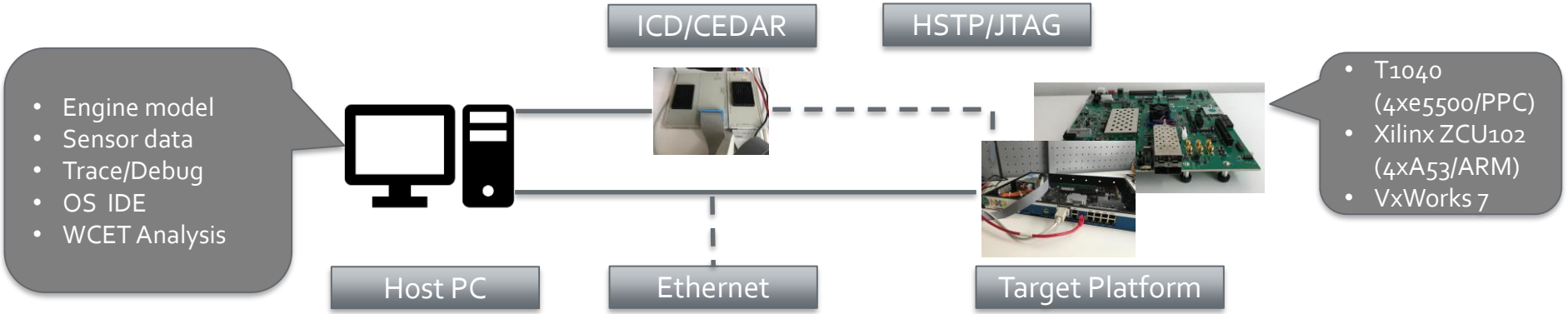
Use Case (WP 5.4B) Starting Point

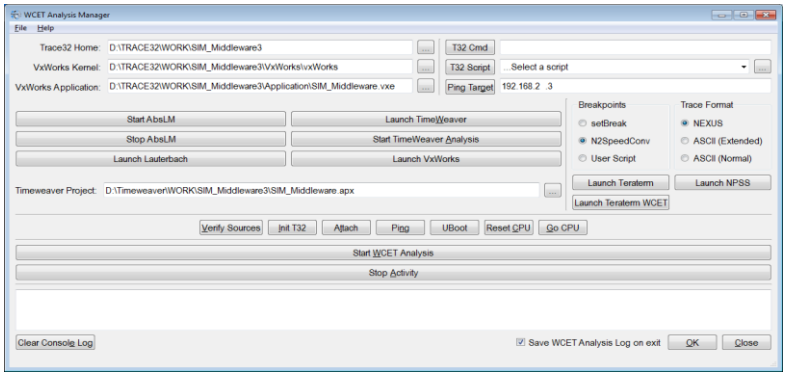
- Aircraft Engine Control Software (ECS) – abstracted product code
- Self-contained single-core generic aviation application that can be run in a PiL (lab ping-pong)/HiL (test rig FADEC) environment
- Available as C code (SCADE KCG generated)
- DO-178C Level A rated software



- 129 subsystems (main control functions), LOC ~150.000
- Cyclic IMA-like static schedule (MIF, MAF). Known execution order on single core
- Validation criteria based on PiL transients

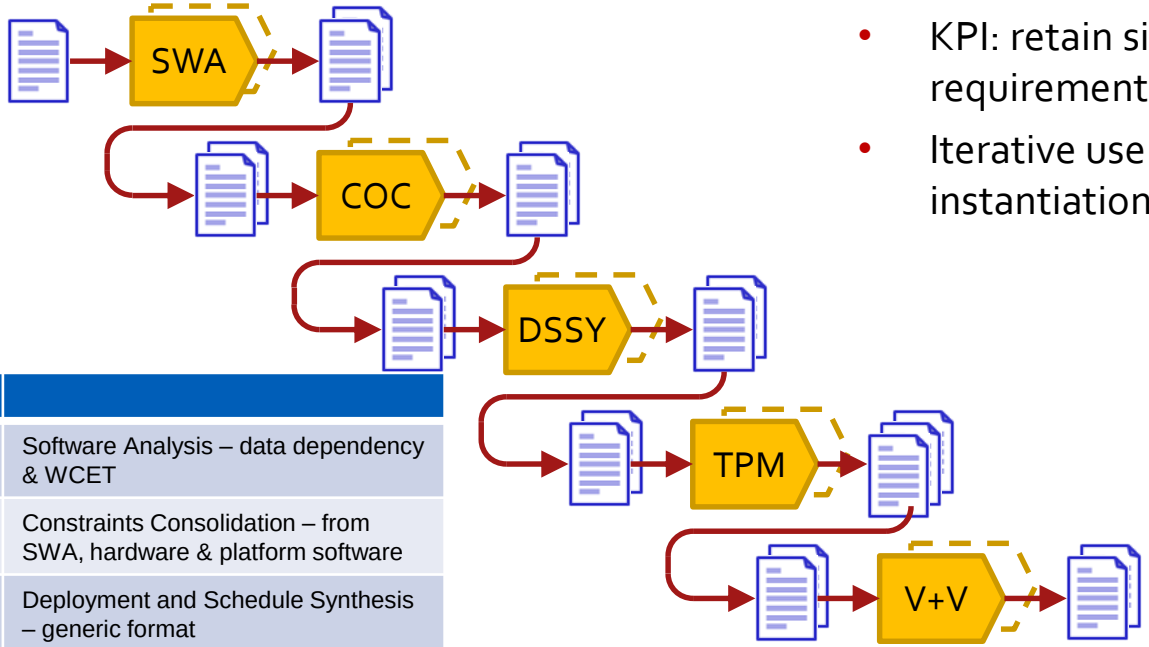
Demonstrator Setup





- Demonstrator Automation
  - Automation of closed loop PiL setup
  - Acquisition of platform data (traces) and engine model transient response
  - WCET analysis
  - Parameter changes (planned)

Process



Acronym	
SWA	Software Analysis – data dependency & WCET
COC	Constraints Consolidation – from SWA, hardware & platform software
DSSY	Deployment and Schedule Synthesis – generic format
TPM	Target Platform Mapping – specific format
V+V	Verification and Validation – timing and functional

Activity

Artefact
Work Product

- KPI: retain single-core behaviour (no formal requirements)
- Iterative use case specific process – instantiation of general process (AP2.2)

Data Dependency Analysis

- Different tools for data dependency analysis are currently investigated
- Instead of using the ECS a smaller subset (ECS_Example) is used (8 subsystems, same data sharing mechanism as ECS, known data dependency, different behavior)

AutoAnalyze

- Static data dependency analysis
- Automotive tool (AUTOSAR) with no native C input. Preprocessing stage (under development) needed
- Preprocessing stage could be replaced by

Gropius

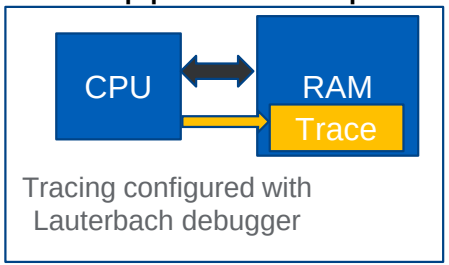
- Static analysis (abstract interpretation)
- Native C input
- First results look promising. Work in progress.

SLX

- Static and dynamic analysis
- First results on static analysis available soon. Work in progress.

WCET Analysis

- Need for an efficient (no source code instrumentation, minimized rig/test bed time) method that supports complex processors
- Short term:
  intrusive



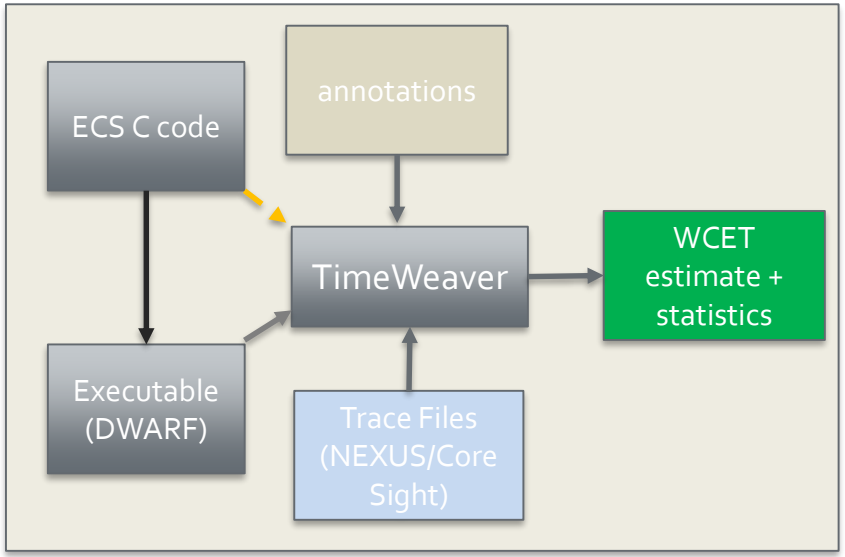
NXP T1040

- Long term (~Q1 2019)
  non-intrusive

AbsInt

ACCEMIC TECHNOLOGIES

Zynq US+



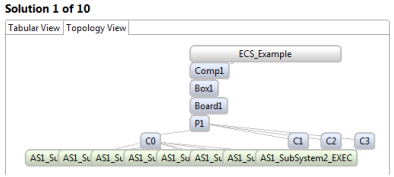
- First results on ECS promising
- Expected speed-up: O (weeks) -> O(hours)
- NDA with AbsInt in place

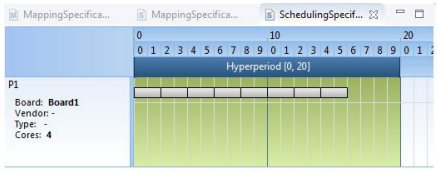
Deployment and Schedule Synthesis

- Deployment and schedule synthesis based on constraints
  - Data dependency between subsystems (atomic units)
  - WCET of subsystems
  - Hardware (interference channels/CAST-32A)
  - Platform software (OS specific)
- Correctness by construction principle (plannable deterministic system)
- Static schedule, run to completion (no preemption)

ASSIST 2.4:

- Valid search based solution (constraint programming)
- Investigated with ECS_Example. Work in progress.

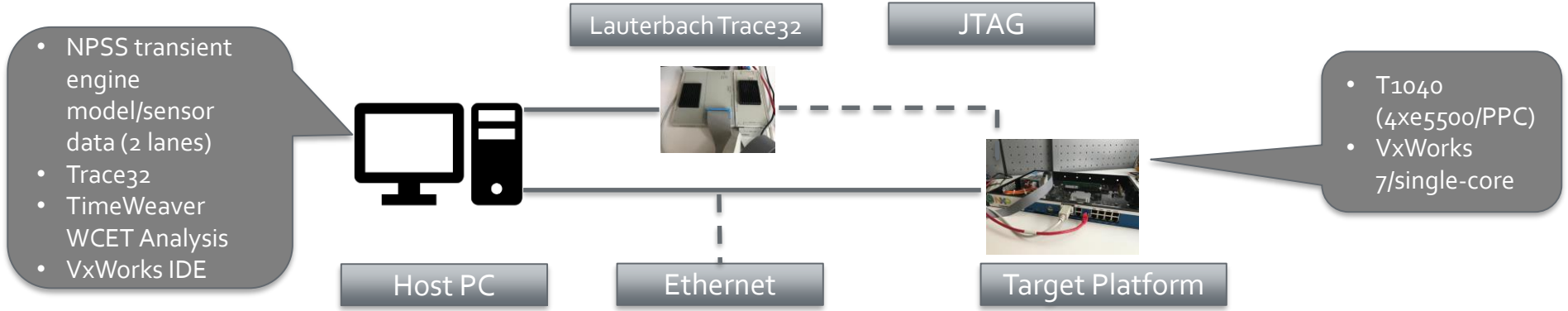




af3:

- Optimized solution (based on SMT solver)
- Will be looked at after ASSIST

Configuration I

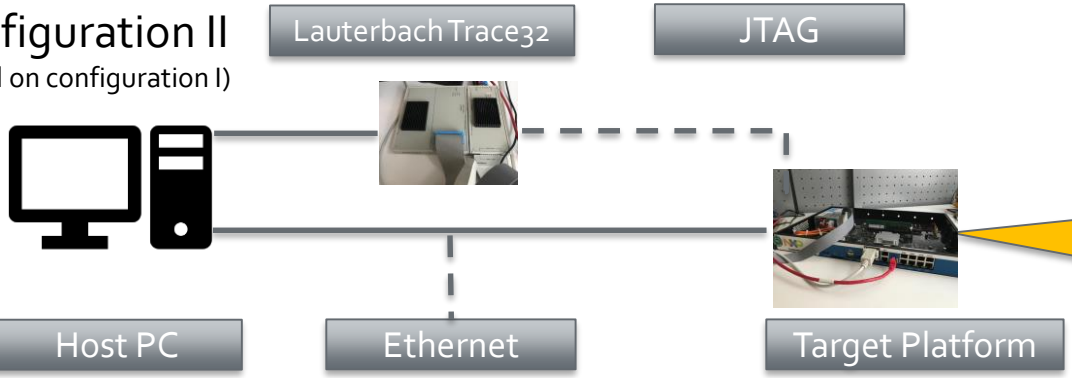


- Single-core setup (VxWorks)
- ECS runs closed loop/30 seconds simulated time
- Traces stored in target RAM (16 MB)/intrusive
- Download via JTAG/NEXUS format
- TimeWeaver analysis

- 129 subsystems take ~30 min
- Results are currently evaluated and problems resolved (7 subsystems fail)
- Evaluation based on different WCET analysis solution

Next Steps – 2018 (WCET Analysis)

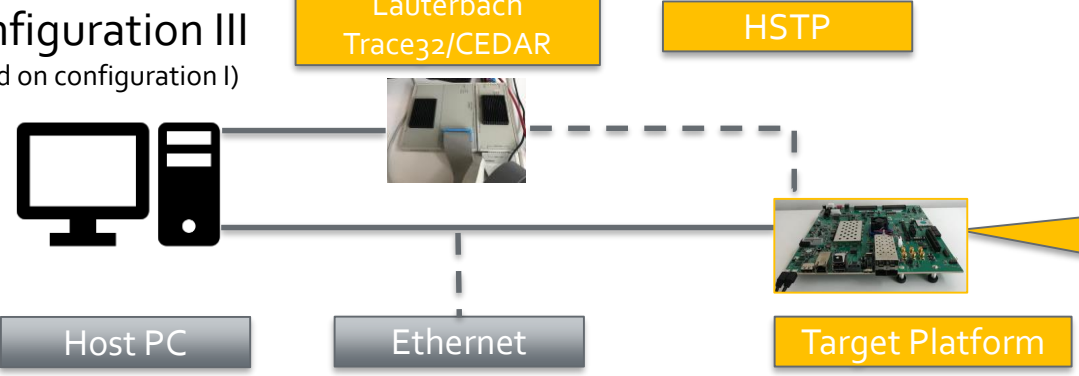
Configuration II
(based on configuration I)



- T1040 (4xe5500/PPC)
- VxWorks 7/quad-core/AS1 pinned to one core

- VxWorks MC configuration
- Probably BMP configuration
- Interference process
- Validation against configuration I

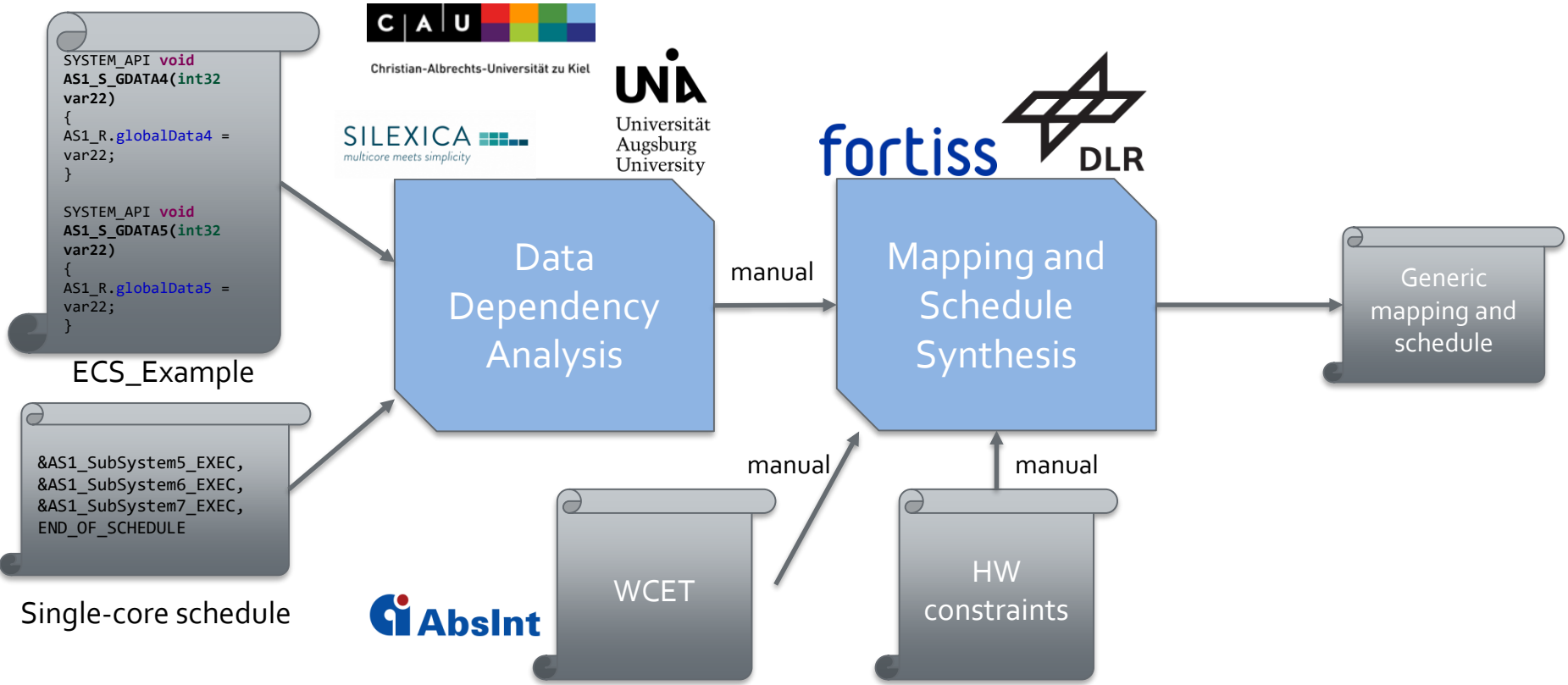
Configuration III
(based on configuration I)



- Xilinx ZCU102 (4xA53/ARM)
- VxWorks 7/quad-core/AS1 pinned to one core

- VxWorks MC configuration
- Probably BMP configuration
- Interference process
- Non-intrusive trace capture
- Validation against configuration I

Next Steps - 2018 (Schedule Synthesis)



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ENTWICKLUNGSPROZESSE I WERKZEUGE I PLATTFORMEN
FÜR SICHERHEITSKRITISCHE MULTICORESYSTEME

STRUCTURED MULTICORE DEVELOPMENT

MULTICORE METHODS AND TOOLS

INDUSTRIAL PLATFORMS FOR MULTICORE SYSTEMS

Thank you for your attention!

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