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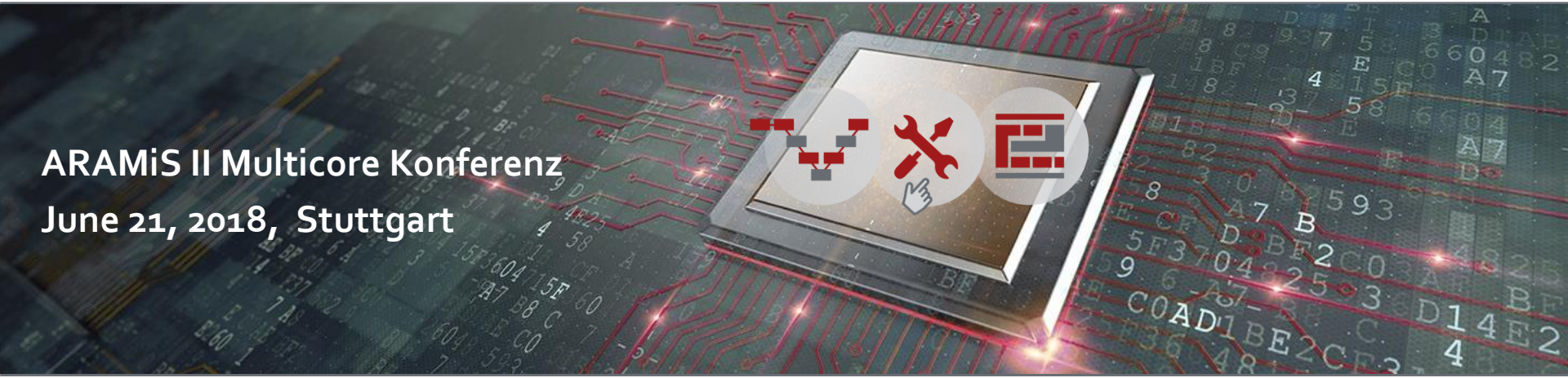
DEVELOPMENT PROCESSES I TOOLS I PLATFORMS
FOR SAFETY-CRITICIAL MULTICORE SYSTEMS



ARAMiS II Multicore Konferenz
June 21, 2018, Stuttgart

Multicore software development

Platform architectures and patterns

Christian Eismann, Elektrobit Automotive GmbH

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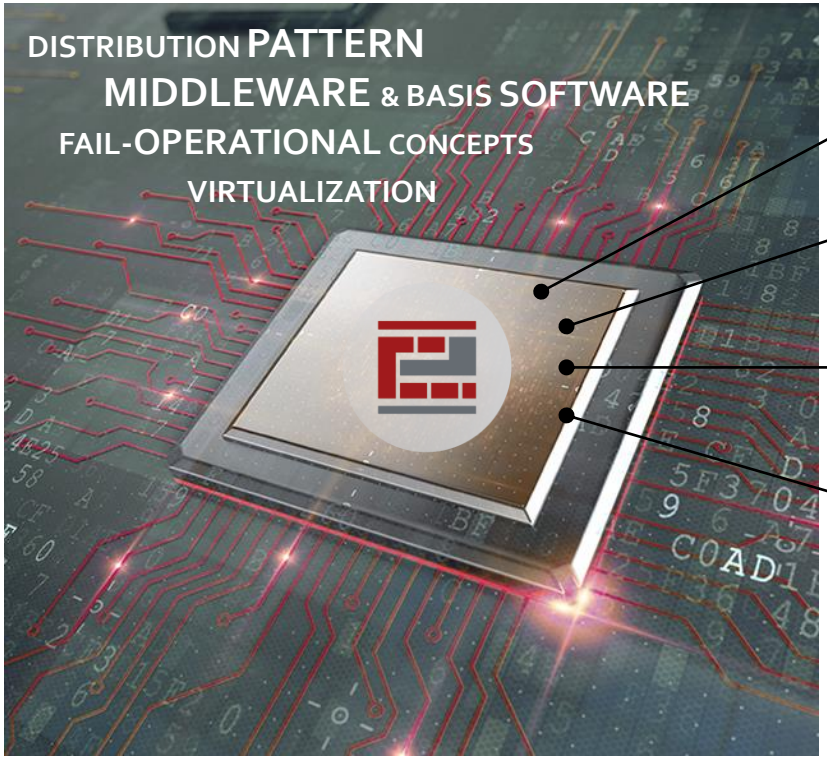
TP4 Industrial Platforms for Multicore Systems



Industrial Platforms for Multicore Systems

Development and extension of established industrial platforms for the use in multicore based systems

Investigation of basis software, middleware and operating systems

Evaluation and development of fail-operational concepts for multicore platforms

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Automotive

Avionics

Industry Automation

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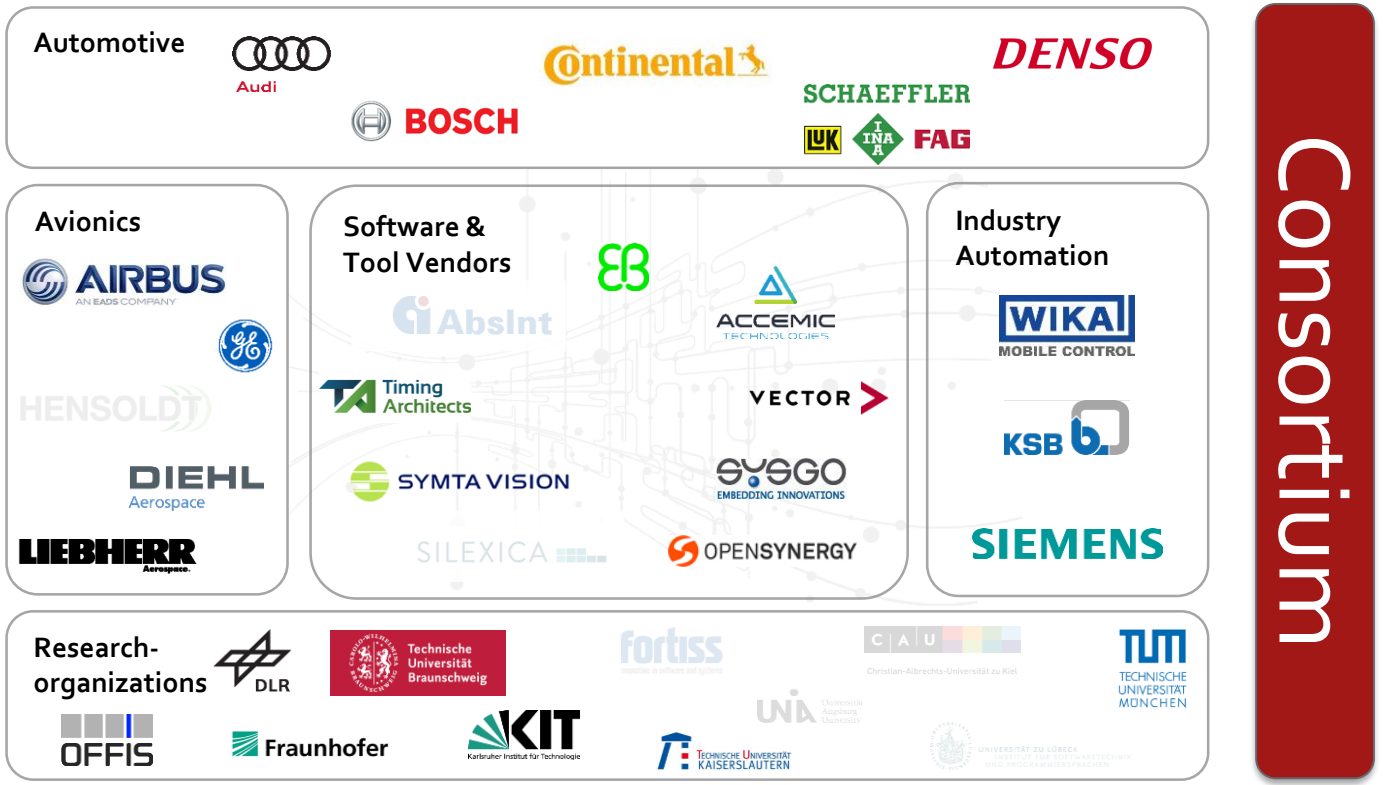

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Platform architecture and distribution patterns

MIDDLEWARE
HIERARCHICAL SCHEDULING
VIRTUALIZATION & HYPERVISORS
COMMUNICATION
BSW DISTRIBUTION
CODE QUALITY

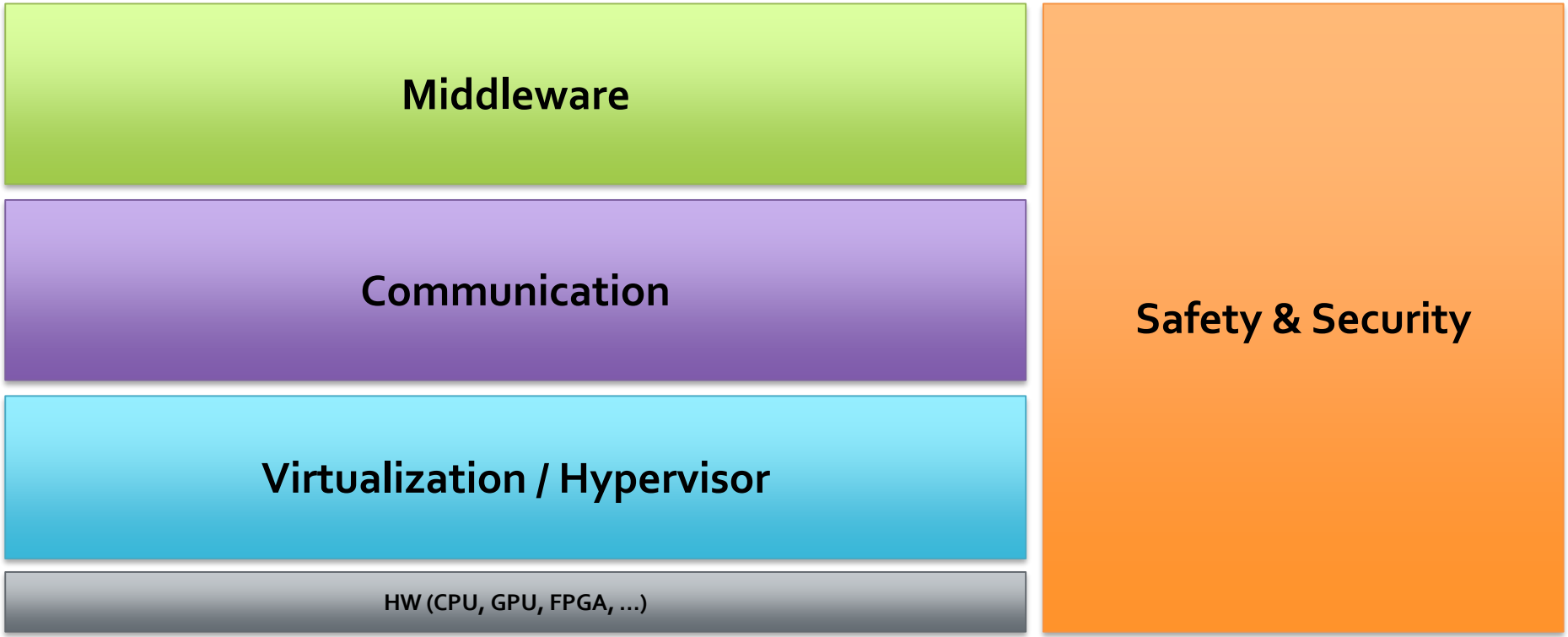
Synchronization and Communication

RESOURCE BROKERING
MIXED CRITICALITY
QUALITY-OF-SERVICE
TIME DIVISION MULTIPLEXING
REAL-TIME
RELIABILITY
NETWORK ON CHIP

Fail-operational concepts

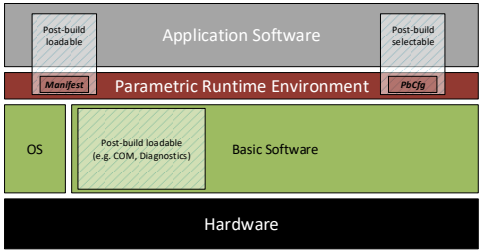
FAILURE MODES
SWITCHOVER MECHANISMS
ISO 26262
FAILURE DIAGNOSIS
SIMPLEX ARCHITECTURE
REDUNDANCY
FAULT TOLERANCE

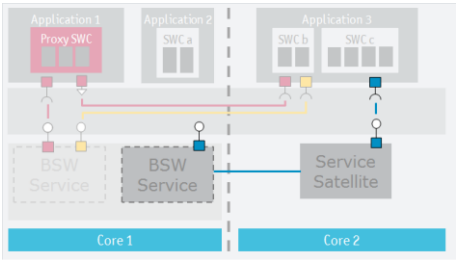
Overview

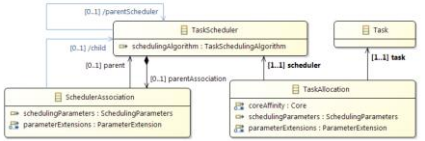

Middleware
Communication
Virtualization / Hypervisor
HW (CPU, GPU, FPGA, ...)
Safety & Security

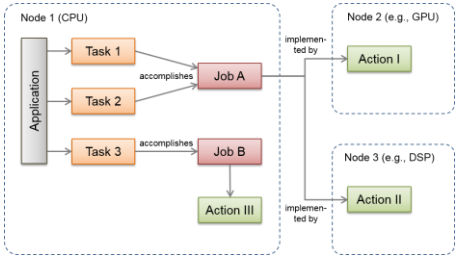
Middleware

- Parametric runtime environment
- Master-satellite pattern
- Hierarchical scheduling
- Task management in heterogeneous systems

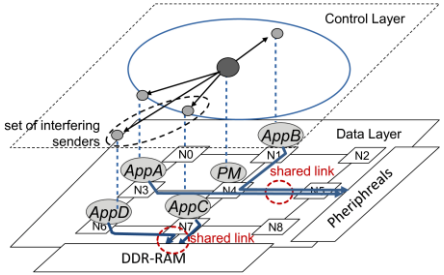


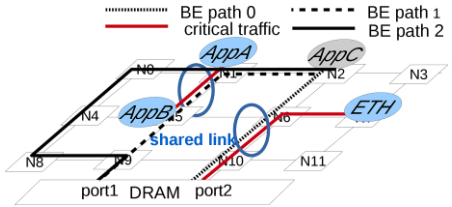


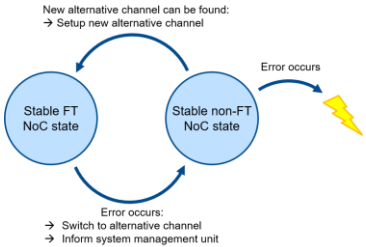




Communication



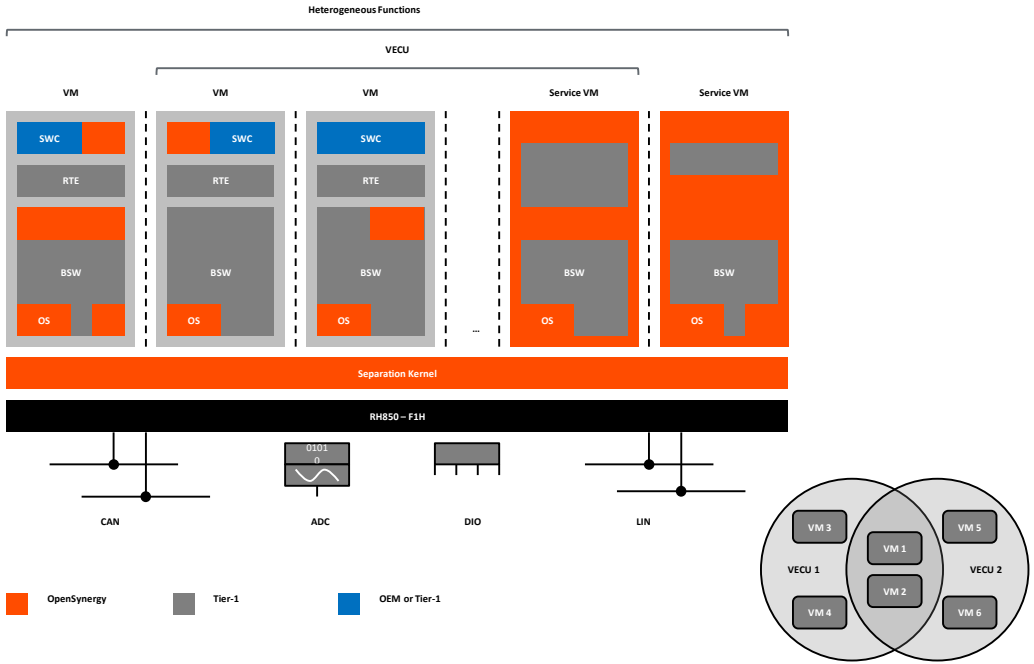


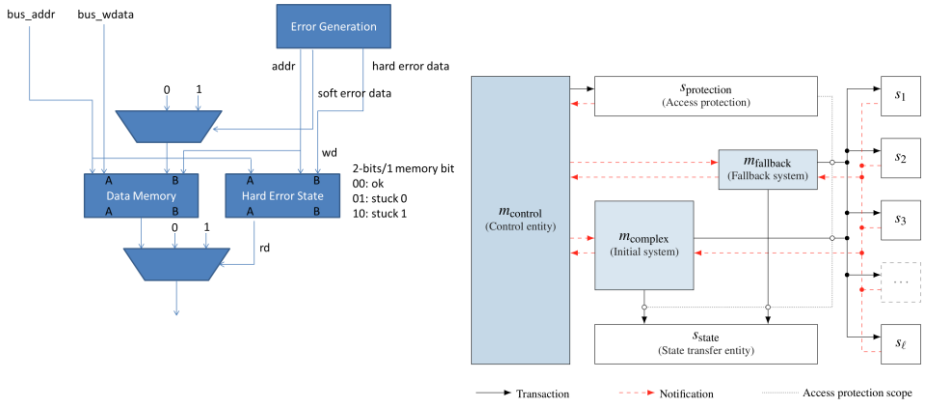


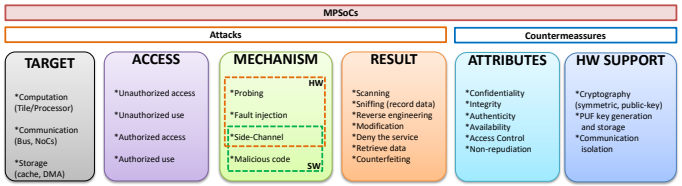
- Communication layer for networks-on-chips
- Communication semantics and model transformation
- Inter-processor communication in heterogeneous architectures
- Fault tolerant communication
- Communication with low latency and real-time requirements

Virtualization / Hypervisor

- Virtualization concepts and hypervisor implementation
- Virtualization of heterogeneous systems
- Online-monitoring of hypervisor operation
- Embedded hypervisor







- Safety assurance and contract based design
- Hypervisor code quality
- Isolated and protected channels inside a chip
- Dynamic migration of functions for heterogeneous SoCs
- Fail-operational switchover mechanisms
- Efficient fail operational multicore processor
- Fail operational concepts for NoC-based multicore systems
- Threat models and mitigation
- Isolated and protected channels inside a chip
- Secure interface to modules outside of a chip

Conclusion

- Successful collaboration between industrial partners and research organizations
- Several scientific publications
- Validation of platform solutions in demonstrators

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ENTWICKLUNGSPROZESSE I WERKZEUGE I PLATTFORMEN
FÜR SICHERHEITSKRITISCHE MULTICORESYSTEME

STRUCTURED MULTICORE DEVELOPMENT

MULTICORE METHODS AND TOOLS

INDUSTRIAL PLATFORMS FOR MULTICORE SYSTEMS

Thank you for your attention!

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